IB915F

Intel® Skylake U

3.5″ Disk Size SBC

USER'S MANUAL

Version 1.0

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Introduction

Product Description

The IB915F is a 3.5-inch single board computer based on the Intel$^{®}$ Skylake U MCP processors.

The IB915F platform is well suited for low-power and high-performance designs in a broad range of markets including Industrial Control & Automation, Digital Signage, Thin Client, Electronic Gaming Machines, and SMB storage appliances.

IB915F Features:

- Supports Intel$^{®}$ 6th generation mobile Core^{TM} i MCP processors
- Two DDR3L SO-DIMM, 1600 MHz, Max. 16GB memory
- Integrated graphics for DisplayPort, LVDS, eDP displays
- 2 x SATA III connector
- 4x COM port connector
- 1 x Mini-PCIe(x1) slot *(w/ USB/mSATA support)*
- 2x GbE (RJ-45) connector
- 1x 9V to 24V DC-IN power connector

Checklist

Your IB915F package should include the items listed below.

- The IB915F SBC
- This User's Manual
- 1 DVD containing chipset drivers and flash memory utility
- Optional cable kit IB75 (containing DC in power cable/PW87, COM port cable / PK1H, SATA & HDD power cable/SATA-26 and USB 2.0 cable/USB-29)
- Other options: Audio-18 audio cable, HSIB915-BGA-A heatsink , HSIB915-BGA-a heat spreader

IB915F Specifications

Product Name	**IB915AF-6600 (Supports iAMT)** **IB915AF-6300 (Supports iAMT)** **IB915F-6100** **IB915F-3955 (MOQ)** ****IB915 will be model name printed on PCB surface****
Form Factor	3.5"
CPU Type	- Intel® 6th generation mobile Core™ i MCP processors (14nm monolithic) - TDP = 15W (DC) , 42mm x 24mm x 1.16mm, FCBGA1356 @ solder side
CPU Speed	Intel® Core™ i7-6600U processor (2.6GHz/3.4GHz) **[IB915AF-6600]** Intel® Core™ i5-6300U processor (2.4GHz/3GHz) **[IB915AF-6300]** Intel® Core™ i3-6100U processor (2.3GHz) **[IB915F-6100](Non-AMT)** Intel® Celeron® 3955U processor (2GHz) **[IB915F-3955](Non-AMT)**
Cache	Up to 4MB
Chipset	Integratd in Intel® 6th Generation Core™ U-series processor
BIOS	AMI BIOS
Memory	Intel® 6th Gen. Core™ U-series processor integrated memory controller - DDR3L(1.35V) @1600 MHz, SO-DIMM x **2 ,** Max.=**16**GB , Non-ECC
Display	Intel® 6th Gen. Core™ U-series processor integrated Gfx, supports 3 independent displays, - eDP x 1 (Thru eDP) - DP++ x 1 (Thru DDI#1) - LVDS(Thru DDI#2, via NXP PTN3460BS/F6)
LAN	1. Intel® I219LM GbE PHY (IB915**A**F-6600 & IB915**A**F-6300) Intel® I219V GbE PHY (IB915F-6100 & IB915F-3955) ** **Thru PCIe port # 9**** 2. Intel® I211AT as 2nd GbE ** **Thru PCIe port # 10****
USB	- Intel® 6th Gen. Core™ U-series processor integrated USB 2.0 host controller ,2 ports onboard pin header + 1 port thru MiniPCIe - Intel® 6th Gen. Core™ U-series processor integrated USB 3.0 host controller **4** x USB 3.0 in the rear panel ** **Thru USB3 port# 1~port# 4 **** - USB 3.1 type C connector thru ASM1142 PCIe to USB 3.1 host controller ** **Thru PCIe port# 1 ****
Serial ATA Ports	Intel® 6th Gen. Core™ U-series processor built-in SATA III controller - 2 x SATA 3.0 (6Gbps) onboard ****Thru SATA port# 0 & port# 2 **** - 1 x mSATA via MiniPCIe full-sized slot ****Thru SATA port# 1/PCIe port # 11****
Audio	Intel® 6th Gen. Core™ U-series processor built-in HD audio controller Realtek ALC662-GR Codec

LPC I/O	Fintek F81846AD-I (128-pin LQFP [14mm x 14 mm]) ▪ COM #1 (RS232/422/485) @ edge I/O With **Fintek F81439N** transceiver x 1 for jumper-less selection ▪ COM #2~COM #4 (RS232 only) [Hardware Monitor] 2 x Thermal inputs 2 x Voltage monitoring
Digital IO	4 in & 4 out
iAMT(11.0)	For IB915AF-6600 & IB915AF-6300
Expansion Slots	1 x mPCIe(x1) w/ USB 2.0 signal, support mSATA [Full-sized] ** Thru PCIe port # 4**
Edge Connector	DP connector x 1 [C12ZZDPP23VD11000P] RJ45 x2 for LAN#1 & #2 (Horizontal Combo type) USB 3.0 stack connector x 2 for USB1/2 & USB3/4 [Blue color] RJ11 x 1 for COM #1 USB 3.1 type C connector x 1
On Board Header/ Connector	DF20-20 socket connector x 2 for 24-bit dual channel LVDS 4 pins box header x 1 for backlight/brightness control eDP 30-pin connector x 1 2 ports x SATA **III** [Blue color] 2x4 pins header x 1 for 2 x USB 2.0 ports[DF11 x 1] DF-11 2x6 pins box header x1 for front audio DF-11 2x5 pins box header x 3 for COM2 ~ COM4 2x5 pins headers x 1 for LPC (Debug purpose only) 4 pins power connector x **1** for SATA HDD 2 pins power connector x 1 for DC-in
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
Power Input	**+9V ~ +24V DC-in**
RoHS	Yes
Board Size	102mm x 147mm
OS support	- Windows 8.1 / Industrial; Windows 10 - Linux - Fedora - Ubuntu
Others	1. Support RAID function 2. iSMART 3.2 3. RTC battery via cable
Optional Cable Kit (IB75)	PW87 x 1 PK1H x 1 SATA-26 x 1 USB29 x 1
Optional items	1. Heatsink 2. Heat Spreader 3. Audio-18 cable (C501AUD1812302000P)

Board Dimensions
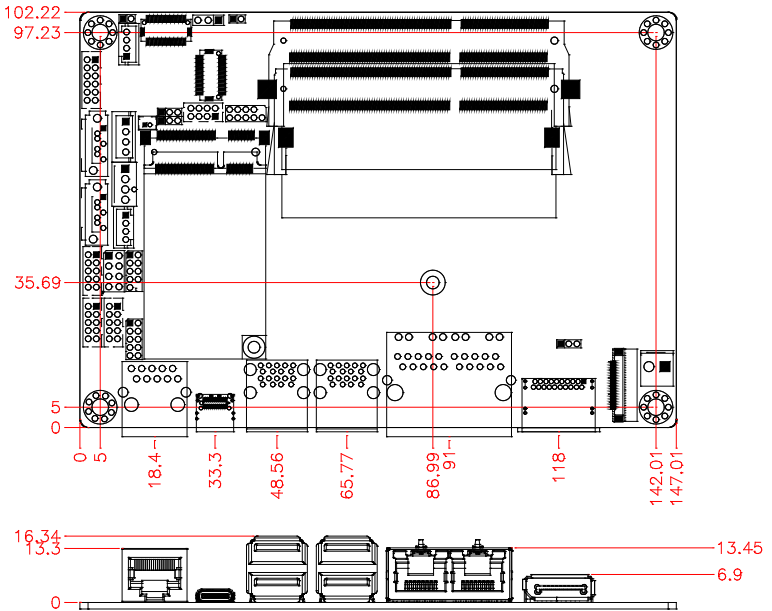
Installations

This section provides information on how to use the jumpers and connectors on the IB915F in order to set up a workable system. The topics covered are:

Installing the Memory

The IB915F board supports two DDR3L memory sockets for a maximum total memory of 16GB DDR3L memory type.

Installing and Removing Memory Modules

To install the DDR3L modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR3L module so that the key of the DDR3L module aligned with that on the memory slot.

2. Gently push the DDR3L module in an upright position until the clips of the slot close to hold the DDR3L module in place when the DDR3L module touches the bottom of the slot.

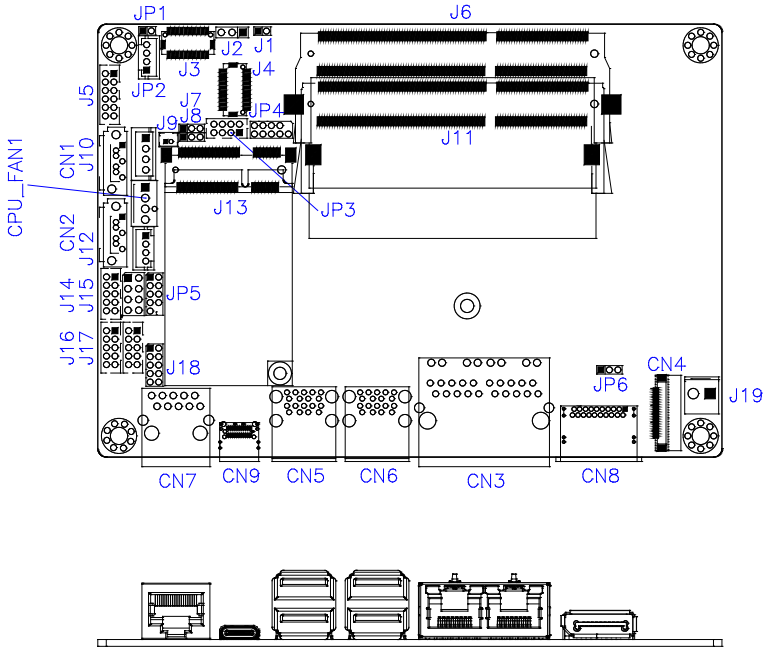3. To remove the DDR3L module, press the clips with both hands.
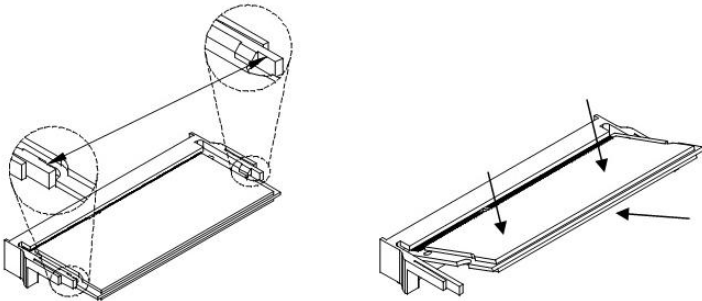
Setting the Jumpers

Jumpers are used on IB915F to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on IB915F and their respective functions.

Jumper Locations on IB915F

JP1: LVDS Panel Brightness Control Selection
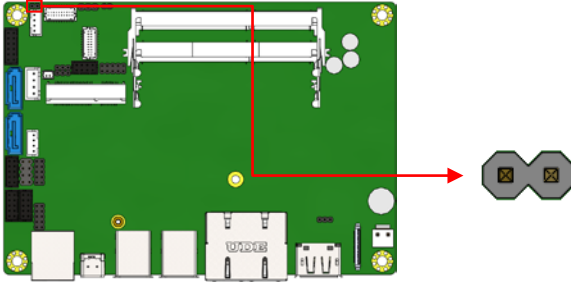
JP1	Brightness Control (PWM mode)
Open	3.3V
Close	5V(Default)

JP2: LCD Backlight Connector
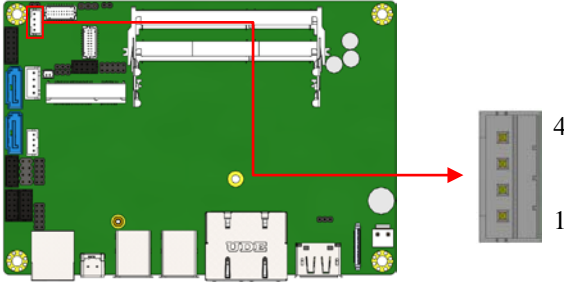
Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Brightness Control
4	Ground

JP3: USB 2.0 Pin Header
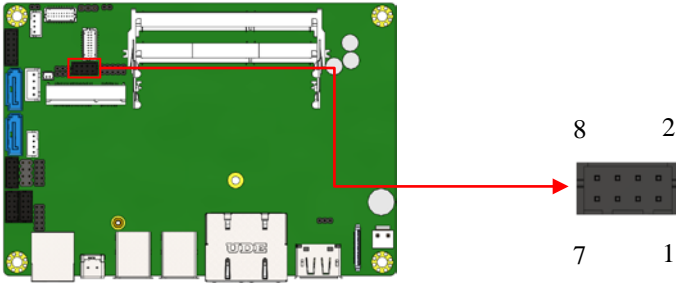
Signal Name	Pin #	Pin #	Signal Name
Vcc	1	2	Ground
D0-	3	4	D1+
D0+	5	6	D1-
Ground	7	8	Vcc

JP4: SPI Flash Connector (Factory use only)
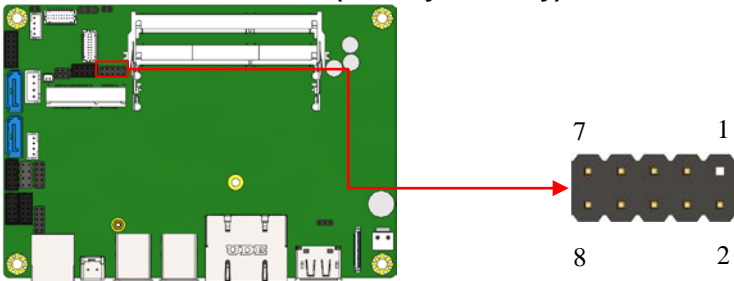
JP5: LPC debug Connector (Factory use only)
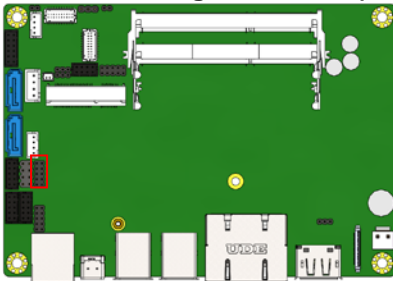
J7: Clear ME
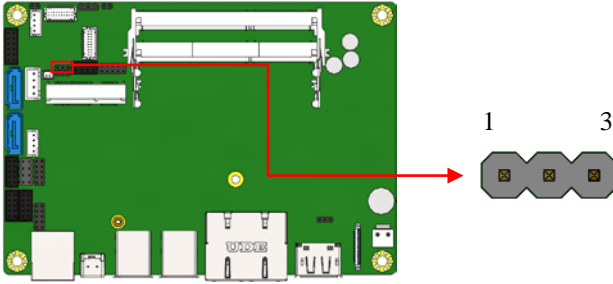
J7	Setting	Function
▢ ▢ ▢ 1 2 3	Pin 1-2 Short/Closed	Normal
▢ ▢ ▢ 1 2 3	Pin 2-3 Short/Closed	Clear ME

J8: Clear CMOS Contents
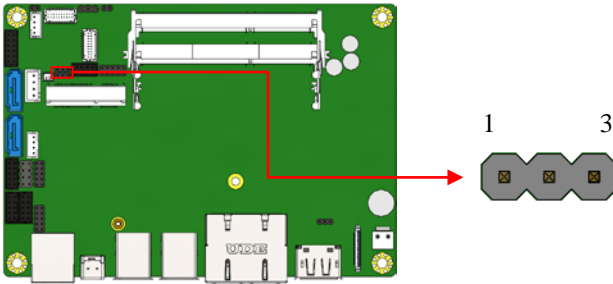
J8	Setting	Function
▢ ▢ ▢ 1 2 3	Pin 1-2 Short/Closed	Normal
▢ ▢ ▢ 1 2 3	Pin 2-3 Short/Closed	Clear CMOS

Connectors on IB915F

Connector Locations on IB915F
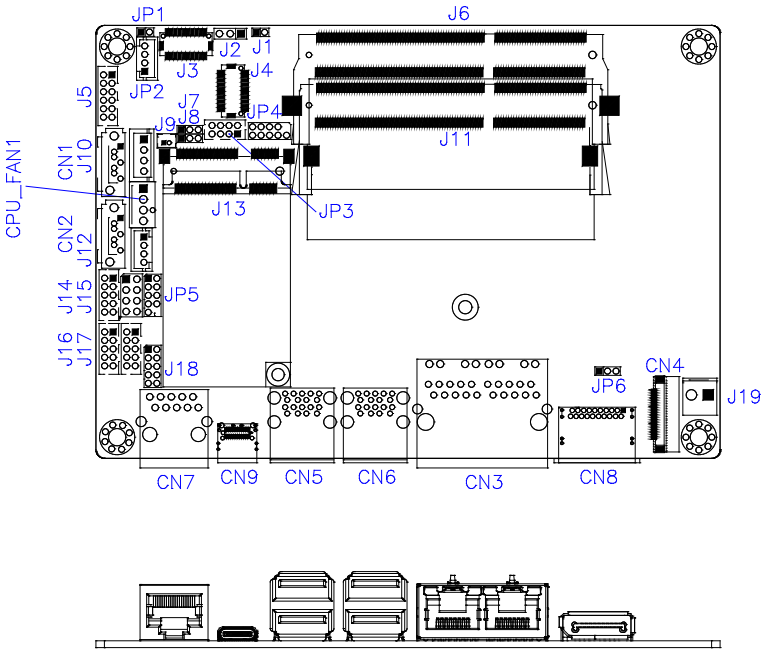
CN1 / CN2: SATA3 Connector
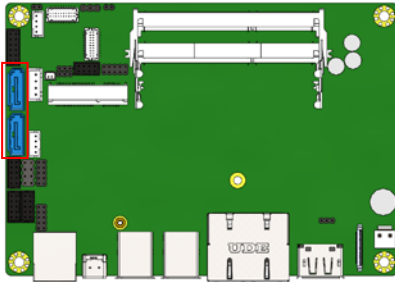
CN3: Gigabit LAN (I219) / Gigabit LAN (I211AT)

CN4: eDP Connector (30 Pin)
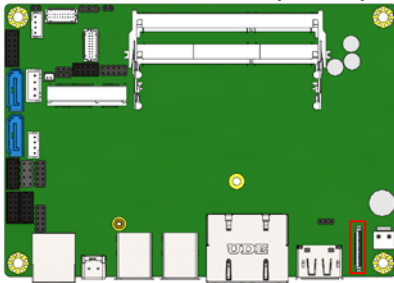
CN5 / CN6: USB3.0 Connector

CN7: COM1 RJ10 Connector

CN8: Display Port Connector

CN9: USB Type C Connector

J1: Flash Descriptor Security Override (Factory use only)
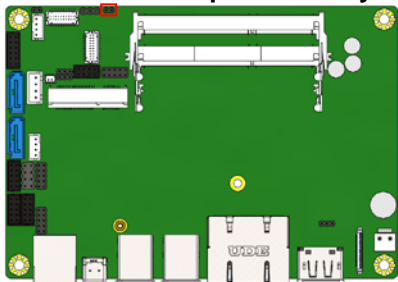
J2/JP6: LVDS Panel Power Selection
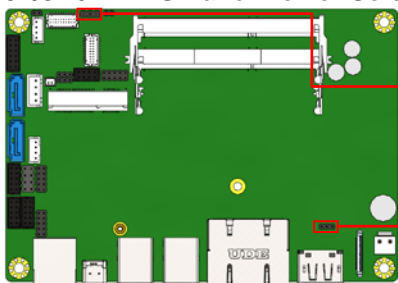
J2/JP6	Setting	Panel Voltage
1 2 3	Pin 1-2 Short/Closed	3.3V (default)
1 2 3	Pin 2-3 Short/Closed	5V

J3, J4: LVDS Connectors (Hirose DF20G-20DP-1V)

J4: First Channel LVDS
J3: Second Channel LVDS
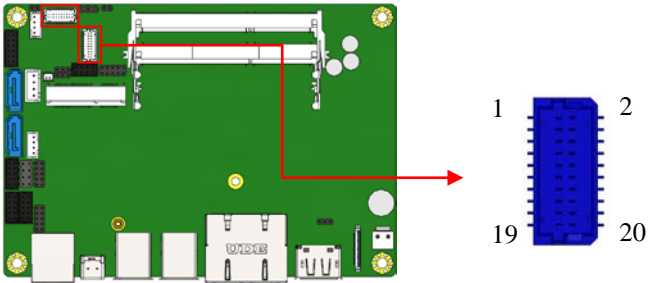
Signal Name	Pin #	Pin #	Signal Name
TX0N	2	1	TX0P
Ground	4	3	Ground
TX1N	6	5	TX1P
Ground	8	7	Ground
TX2N	10	9	TX2P
Ground	12	11	Ground
CLKN	14	13	CLKP
Ground	16	15	Ground
TX3N	18	17	TX3P
Power	20	19	Power

J5: Audio Connector (DF11-12DP-2DSA)
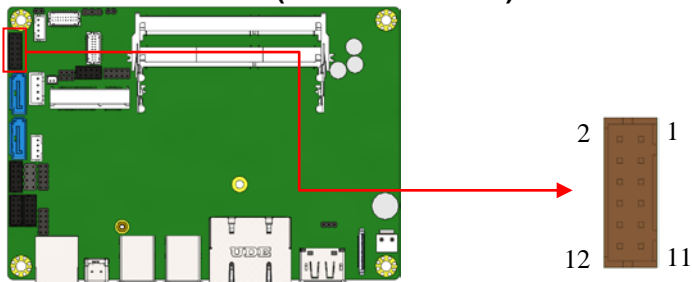
Signal Name	Pin #	Pin #	Signal Name
LINEOUT_R	2	1	LINEOUT_L
Ground	4	3	JD_FRONT
LINEIN_R	6	5	LINEIN_L
Ground	8	7	JD_LINEIN
MIC-R	10	9	MIC_L
Ground	12	11	JD_MIC1

J11: DDR3L SO-DIMM (CH-A) Socket
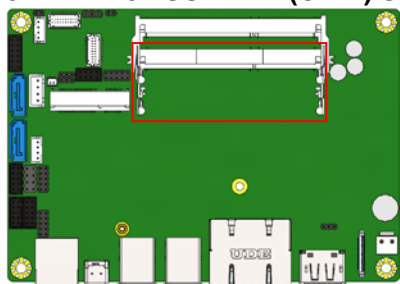
J6: DDR3L SO-DIMM (CH-B) Socket
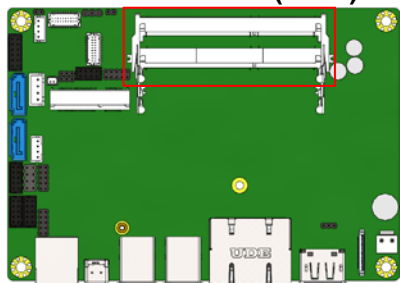
J9: Battery Connector
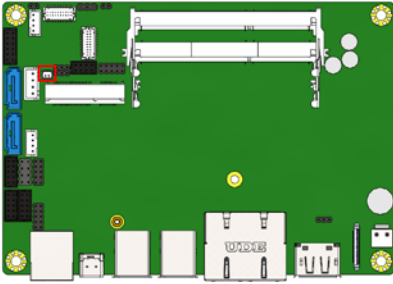
J10: SATA HDD Power Connectors
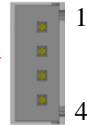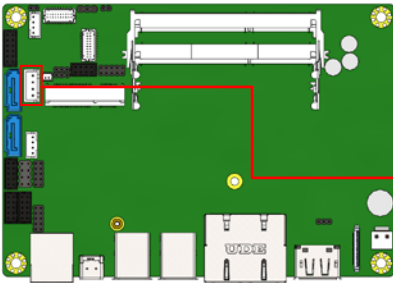
Pin #	Signal Name
1	+5V
2	Ground
3	Ground
4	+12V

J12: MCU JTAG
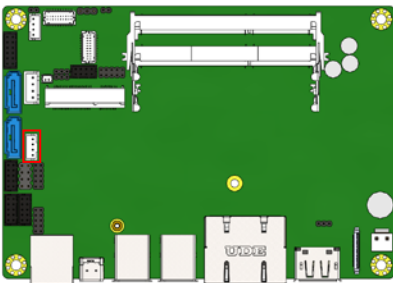
J13: Mini PCIE / mSATA Slot
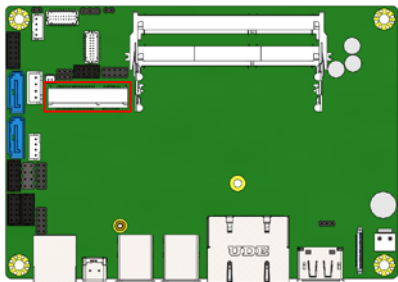
J14, J17: COM3/COM4

J15: Front Panel

```
1 □ □ 2
  □ □
  □ □
7 □ □ 8
```
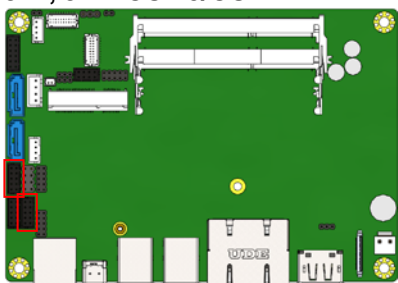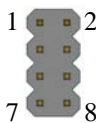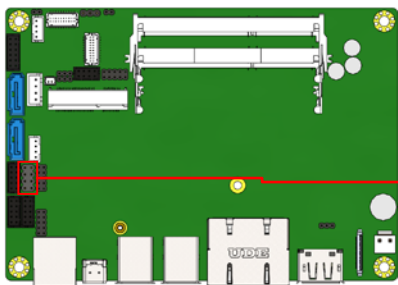
Signal Name	Pin #	Pin #	Signal Name
GND	1	2	PWR_BTN
3.3V	3	4	HDD Active
GND	5	6	Reset
+5V	7	8	GND

J16: COM2
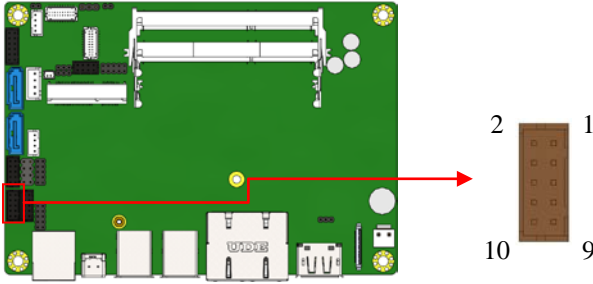
Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	2	RXD, Receive data
TXD, Transmit data	3	4	DTR, Data terminal ready
GND, ground	5	6	DSR, Data set ready
RTS, Request to send	7	8	CTS, Clear to send
RI, Ring indicator	9	10	Not Used

J18: Digital I/O
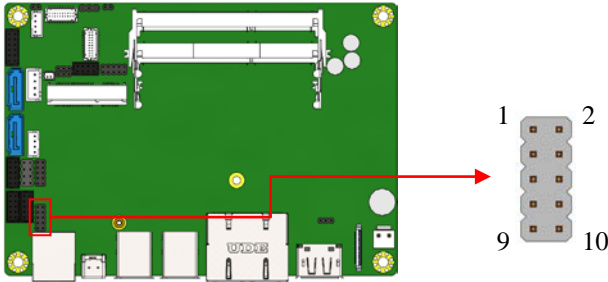
Signal Name	Pin #	Pin #	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J19: DC_IN Connector

2   1
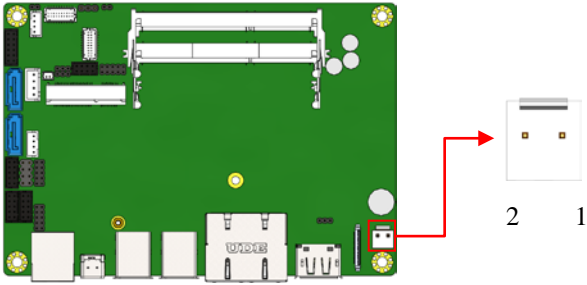
Pin #	Signal Name
1	+9V or +24V
2	GND

BIOS Setup

This chapter describes the different settings available in the BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also adds virus and password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

```
Press  <DEL> or <ESC>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Main Settings

Main Advanced	Chipset	Boot	Security	Save & Exit
				Choose the system default language
Access Level		Administrator		
Total memory		4096 MB		
Memory Frequency		1600 Mhz		→ ←**Select Screen**
System Language		[Englisg]		↑↓ **Select Item**
				Enter: Select
				+- Change Field
System Date		[Tue 10/29/2013]		**F1: General Help**
System Time		[15:27:20]		**F2: Previous Values**
				F3: Optimized Default
				F4: Save
				ESC: Exit

System Date
Set the Date. Use Tab to switch between Data elements.

System Time
Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility – Copyright © 2016 American Megatrends, Inc.

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

```
► ACPI Settings
► LVDS (eDP/DP) Configuration          → ←Select Screen
► ISmart Controller
► AMT Configuration                     ↑↓ Select Item
► Fintek Super IO Configuration        Enter: Select
► Hardware Monitor                     +-  Change Field
► CPU Configuration                    F1: General Help
► SATA Configuration                   F2: Previous Values
► Acoustic Management Configuration    F3: Optimized Default
► Network Stack Configuration          F4: Save
► CSM Configuration                    ESC: Exit
► USB Configuration
```

ACPI Settings

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

ACPI Settings		
		→ ←Select Screen
Enable ACPI Auto Configuration	[Disabled]	↑↓ Select Item
		Enter: Select
Enable Hibernation	[Enabled]	+- Change Field
ACPI Sleep State	[S3 (Suspend to R…)]	F1: General Help
Lock Legacy Resources	[Disabled]	F2: Previous Values
S3 Video Report	[Disabled]	F3: Optimized Default
ACPI Low Power S0 Idle	[Disabled]	F4: Save
		ESC: Exit

Enable Hibernation

Enables or Disables System ability to hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State

Select ACPI sleep state the system will enter, when the SUSPEND button is pressed.

Lock Legacy Resources

Enabled or Disabled Lock of Legacy Resources.

S3 Video Report

Enabled or Disabled S3 Video Report.

ACPI Low Power S0 Idle

Enabled or Disabled ACPI Low Power S0 Idle Support.

LVDS (eDP/DP) Configuration

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Main	Advanced	Chipset	Boot	Security	Save & Exit

LVDS (eDP/DP) Configuration

LVDS (eDP/DP) Support   [Enabled]
Panel Color Depth   [18 BIT]
LVDS Channel Type   [Single]
Panel Type   [800 x 600]
Brightness Control   [Enabled]
Signal Type   [PWM]
Brightness Percent   [100%]
PWM Clock   [200Hz]

→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-   Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save & Exit
ESC: Exit

Panel Color Depth
Select the LFP Panel Color Depth: 18 Bit, 24 Bit.

LVDS Channel Type
Select LVDS Channel Type

Panel Type
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item: 800x600 LVDS ~ 1920x1080 LVDS.

LVDS Brightness Control
Enable or Disable LVDS Brightness

ISmart Controller

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Main	**Advanced**	Chipset	Boot	Security	Save & Exit

ISmart Controller

Power-On after Power failure [Disable]
Temperature Gurdian   [Disable]
Schedule Slot 1   [None]
Schedule Slot 2   [None]

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save
ESC: Exit
```

Power-On after Power failure
Enable or Disable.

Temperature Gurdian
Enable or Disable.

Schedule Slot 1 / 2
Setup the hour/minute for system power on.

AMT Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit

Intel AMT	[Enabled]	
BIOS Hotkey Pressed	[Disabled]	
MEBx Selection Screen	[Disabled]	
Hide Un-Configure ME Confirmation	[Disabled]	
Amt Wait Timer	0	→ ←Select Screen
ASF	[Enabled]	↑↓ Select Item
Activate Remote Assistance Process	[Disabled]	Enter: Select
USB Configure	[Enabled]	+- Change Field
PET Progress	[Enabled]	F1: General Help
AMT CIRA Timeout	0	F2: Previous Values
Watchdog	[Disabled]	F3: Optimized Default
OS Timer	0	F4: Save
BIOS Timer	0	ESC: Exit

AMT Configuration

This configuration is supported only with IB915AF(with iAMT function).
Options are Enabled and Disabled.
Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

Amt Wait Timer

Set timer to wait before sending ASF_GET_BOOT_OPTIONS.

Activate Remote Assistance Process

Trigger CIRA boot.

PET Progress

User can Enable/Disable PET Events progress to receive PET events or not.

Watchdog Timer

Enable/Disable Watchdog Timer.

Fintek Super IO Configuration

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

Fintek Super IO Configuration		→ ←Select Screen
		↑↓ Select Item
Super IO Chip	F81846 Serial	Enter: Select
► Serial Port 1 Configuration		+- Change Field
► Serial Port 2 Configuration		F1: General Help
► Serial Port 3 Configuration		F2: Previous Values
► Serial Port 4 Configuration		F3: Optimized Default
		F4: Save
		ESC: Exit

Serial Port Configuration
Set parameters of serial ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

Hardware Monitor

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Main	**Advanced**	Chipset	Boot	Security	Save & Exit

PC Health Status		→ ←Select Screen
		↑↓ Select Item
CPU temperature	:+46 C	Enter: Select
System temperature	:+46 C	+- Change Field
VCore	:+0.888 V	F1: General Help
VBAT	:+3.248 C	F2: Previous Values
		F3: Optimized Default
CPU Shutdown Temperature	[Disabled]	F4: Save
		ESC: Exit

CPU Shutdown Temperature
The default setting is Disabled.

Temperatures/Voltages
These fields are the parameters of the hardware monitoring function feature of the board. The values are read-only values as monitored by the system and show the PC health status.
[

CPU Configuration

This section shows the CPU configuration parameters.

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Main	Advanced	Chipset	Boot	Security	Save & Exit

CPU Configuration		
Intel(R) CPU Core(TM)i3-6100U CPU @ 2.30GHz		
CPU Signature	406E3	
Microcode Patch	33	
Processor cores	2	
Max CPU Speed	2200 MHz	
Min CPU Speed	500 MHz	
CPU Speed	3100 MHz	
Processor Cores	2	
Hyper Threading Technology	Supported	
Intel VT-x Technology	Supported	
Intel SMX Technology	Not Supported	
64-bit	Supported	
EIST Technology	Supported	
CPU C3 State	Supported	
CPU C6 State	Supported	
CPU C7 State	Supported	
		→ ←Select Screen
Intel (R) SpeedStep(tm)-	[Enabled]	↑↓ Select Item
Turbo Mode	[Enabled]	Enter: Select
Package power Limit MSR Lock	[Disabled]	+- Change Field
1-Core Ratio Limit Override	0	F1: General Help
2-Core Ratio Limit Override	0	F2: Previous Values
Configurable TDP Boot Mode	[Nominal]	F3: Optimized Default
Configurable TDP Lock	[Disabled]	F4: Save
CTDP BIOS control	[Disabled]	ESC: Exit
PRMRR Size	[AUTO]	

Intel (R) SpeedStep(tm)

Allows more than two frequency ranges to be supported.

Turbo Mode

Enable or Disable Turbo Mode.

Package power Limit MSR Lock

Enable/disable locking of Package Power Limit settings.When enabled, PACKAGE_POWER_LIMIT MSR will be locked and a rest will be required to unlock the register.

Configurable TDP Boot Mode

Configurable TDP Boot Mode as Nominal/Up/Down/Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero.

Configurable TDP Lock

Configurable TDP Lock sets the Lock bits on TURBO_ACTIVATION_RATIO and CONFIG_TDP_CONTROL. Note: When CTDP Lock is enabled Custom ConfigTDP Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0.

CTDP BIOS control

Enables CTDP control viaruntime ACPI BIOS methods. This "BIOS only" feature does not require EC or driver support.

SATA Configuration

SATA Devices Configuration.

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Main	**Advanced**	Chipset	Boot	Security	Save & Exit

```
   SATA Controller(s)                    [Enabled]
   SATA Mode Selection                   [AHCI]
►  Software Feature Mask Configuration
   Aggressive LPM Support                [Enabled]


   Serial ATA Port 0                     [Empty]
     Software Preserve                   [Unknown]
     Port 0                              [Enabled]
     Hot Plug                            [Disabled]
   Serial ATA Port1                      [Empty]         → ←Select Screen
     Software Preserve                   [Unknown]
     Port 1                              [Enabled]       ↑↓ Select Item
     Hot Plug                            [Disabled]      Enter: Select
   Serial ATA Port2                      [Empty]         +-  Change Field
     Software Preserve                   [Unknown]       F1: General Help
     Port 2                              [Enabled]       F2: Previous Values
     Hot Plug                            [Disabled]      F3: Optimized Default
   Serial ATA Port3                      [Empty]         F4: Save
     Software Preserve                   [Unknown]       ESC: Exit
     Port 3                              [Enabled]
     Hot Plug                            [Disabled]
```

SATA Controller(s)

Enable / Disable Serial ATA Controller.

SATA Mode Selection

(1) AHCI Mode.
(2) RAID Mode.

Software Feature Mask Configuration

RAID OROM/RST driver will refer to the SWFM configuration to enable or diable the storage features.

Aggressive LPM Support

Enable PCH to aggressively enter link power state.

Acoustic Management Configuration

Main	**Advanced**	Chipset	Boot	Security	Save & Exit
Acoustic Management Configuration				→ ←Select Screen	
HDD not found				↑↓ Select Item	
				Enter: Select	
				+- Change Field	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Default	
				F4: Save	
				ESC: Exit	

Acoustic Management Configuration

Option to Enable or Disable Automatic Acoustic Management

Network Stack Configuration

Main	**Advanced**	Chipset	Boot	Security	Save & Exit
				→ ←Select Screen	
Network Stack		[Disabled]		↑↓ Select Item	
				Enter: Select	
				+- Change Field	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Default	
				F4: Save	
				ESC: Exit	

Network Stack Configuration

Network Stack Settings.

CSM Configuration

Main	Advanced	Chipset	**Boot**	Security	Save & Exit

Compatibility Support Module Configuration

CSM Support	Enabled
CSM16 Module Version	07.78
GateA20 Active	[Upon Request]
Option ROM Messages	[Force BIOS]
INT19 Trap Response	[Immediate]
Boot option filter	[UEFI and Legacy]
Option ROM execution	
Network	[Do not launch]
Storage	[Legacy]
Video	[Legacy]
Other PCI device	[Legacy]

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save
ESC: Exit
```

CSM Support
Enable/Disable CSM Support.

Boot option filter
This option controls what devices system can boot to.

Network
Controls the execution of UEFI and Legacy PXE OpROM.

Storage
Controls the execution of UEFI and Legacy Storage OpROM.

Video
Controls the execution of UEFI and Legacy Video OpROM.

Other PCI device
Determines OpROM execution policy for devices other than Network, Storage, or Video.

USB Configuration

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

USB Configuration

USB Module Version   12

USB Controllers:
     1 XHCI
USB Devices:
     1 Keyboard, 1Mouse

Legacy USB Support	[Enabled]
XHCI Hand-off	[Disabled]
USB MASS Storage Driver Support	[Enabled]
Port 60/64 Emulation	[Enabled]
USB hardware delays and time-outs:	
USB Transfer time-out	[20 sec]
Device reset tine-out	[20 sec]
Device power-up delay	[Auto]

→ ←Select Screen
↑↓ Select Item
Enter: Select
+-　Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save
ESC: Exit

Legacy USB Support

Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected.
DISABLE option keeps USB devices available only for EFI applications.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

USB Mass Storage Driver Support

Enable/Disable USB Mass Storage Driver Support.

Port 60/64 Emulation

Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware 0Ses.

USB Transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

Device reset time-out

USB mass Storage device start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

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Main	Advanced	Chipset	Boot	Security	Save & Exit

► System Agent (SA) Configuration
► PCH-IO Configuration

System Agent (SA) Configuration

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Main	Advanced	Chipset	Boot	Security	Save & Exit

System Agent Bridge Name	Skylake
System Agent RC Version	1.6.0.0
VT-d Capability	Supported
VT-d	[Enabled]
eDRAM Mode	[eDRam HW Mode]

► Graphics Configuration

```
→ ←Select Screen
↑↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

VT-d

VT-d capability.

eDRAM Mode

SW Mode eDRAM on or eDRAM off.

PCH-IO Configuration

This section allows you to configure the North Bridge Chipset.

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Main	Advanced	Chipset	Boot	Security	Save & Exit
Intel PCH RC Version		1.6.0.0			
Intel PCH SKU Name		PCH-LP Mobile (U) Pre…			
Intel PCH Rev ID		21/C1			
					→ ← Select Screen
PCH LAN Controller		[Enabled]			↑↓ Select Item
LAN PHY Drives LAN_WAKE#		[Disabled]			Enter: Select
Sensor Hub Type		[None]			+- Change Field
LAN Wake From DeepSx		[Enabled]			F1: General Help
Wake on LAN		[Enabled]			F2: Previous Values
SLP_LAN# Low on DC Power		[Enabled]			F3: Optimized Default
					F4: Save
					ESC: Exit

PCH LAN Controller

Enable or disable onboard NIC.

LAN PHY Drives LAN_WAKE#

Enables/Disables LAN Phy driving LAN_WAKE# else platform drives LAN_WAKE#.

Sensor Hub Type

Choose the senor Hub Type, 'None' will Suppress 'I2C Sensor Hub' Setup option','I2C' Will Suppress'ALS' Setup option and 'USB' will Suppress Both I2C and ALS.

LAN Wake From DeepSx

Wake from DeepSx by the assertion of LAN_WAKE# pin.

Wake on LAN

Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

SLP_LAN# Low on DC Power

Enable/Disable SLP_LAN# Low on DC Power

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

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Main	Advanced	Chipset	Boot	Security	Save & Exit

```
Password Description


If ONLY the Administrator's password is set, then
this only limit access to Setup and is only asked for
when entering Setup.
If ONLY the User's password is set, then this is a
power on password and must be entered to boot or
enter Setup. In Setup the User will have              → ←Select Screen
Administrator rights
                                                      ↑↓ Select Item
The password length must be
                                                      Enter: Select
in the following range:
                                                      +-  Change Field
Minimum length                          3
                                                      F1: General Help
Maximum length                          20
                                                      F2: Previous Values
                                                      F3: Optimized Default
Administrator Password
                                                      F4: Save
User Password
                                                      ESC: Exit
```

Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Boot Settings

This section allows you to configure the boot settings.

Main	Advanced	Chipset	**Boot**	Security	Save & Exit

Boot Configuration	
Setup Prompt Timeout	1
Bootup NumLock State	[On]
Quiet Boot	[Disabled]
Fast Boot	[Disabled]
Boot mode select	[LEGACY]
FIXED BOOT ORDER Priorities	
Boot Option #1	[Hard Disk]
Boot Option #2	[CD / DVD]
Boot Option #3	[USB Hard Disk]
Boot Option #4	[USB CD / DVD]
Boot Option #5	[USB Key]
Boot Option #6	[USB Floppy]
Boot Option #7	[USB LAN]
Boot Option #8	[Network]

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save
ESC: Exit
```

Setup Prompt Timeout

Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

Enables/Disables Quiet Boot option.

Fast Boot

Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Boot mode select

Select boot mode LEGACY/UEFI

FIXED BOOT ORDER Priorities

Sets the system boot order.

Save & Exit Settings

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Main	**Advanced**	Chipset	Boot	Security	Save & Exit

```
Save Changes and Exit
Discard Changes and Exit
Save Changes and Reset
Discard Changes and Reset
                                          → ←Select Screen
Save Options                              ↑↓ Select Item
Save Changes                              Enter: Select
Discard Changes                           +-  Change Field
                                          F1: General Help
Restore Defaults                          F2: Previous Values
Save as User Defaults                     F3: Optimized Default
Restore User Defaults                     F4: Save
                                          ESC: Exit
```

Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.
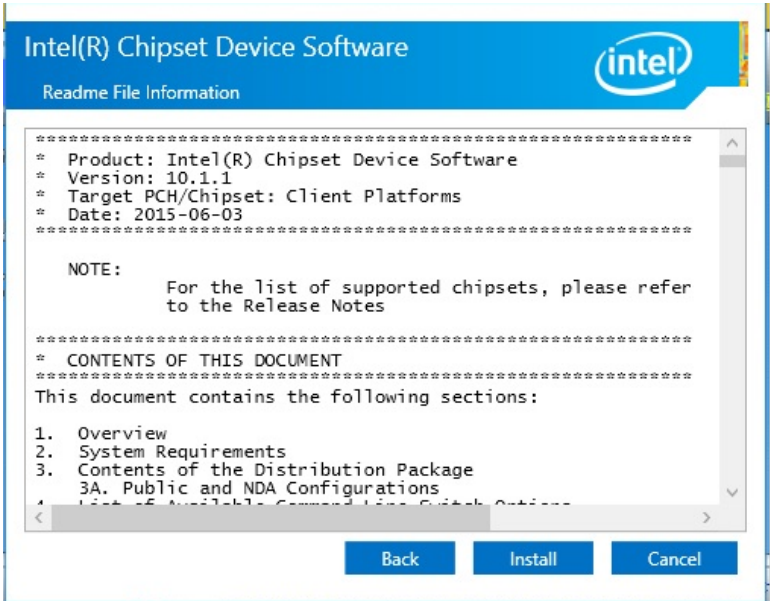
1. Insert the DVD that comes with the board. Click *Intel* and then *Intel(R) Skylake-U Chipset Drivers*.

2. Click *Intel(R) Chipset Software Installation Utility.*

3. When the Welcome screen to the Intel® Chipset Device Software appears, click *Next* to continue.

4. Click *Yes* to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click *Install* to continue the installation.

6. The Setup process is now complete. Click *Finish* to restart the computer and for changes to take effect.

VGA Drivers Installation

1. Insert the DVD that comes with the board. Click **Intel** and then **Intel(R) Skylake-U Chipset Drivers**.

2. Click **Intel(R) HD Graphics Driver.**

3. When the Welcome screen appears, click *Next* to continue.

4. Click *Yes* to to agree with the license agreement and continue the installation.
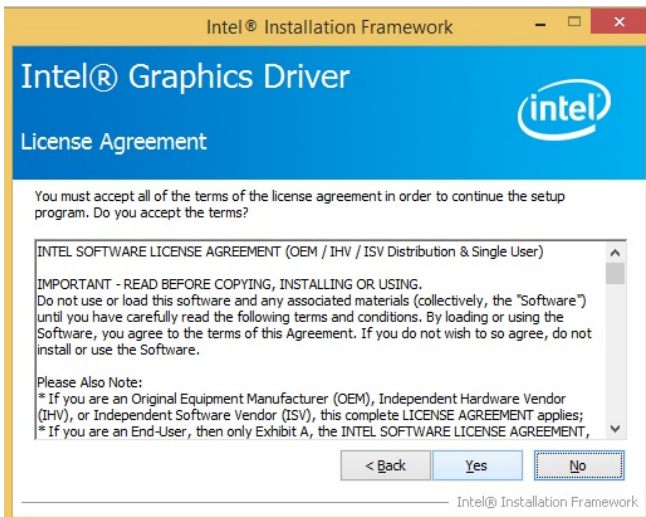
5. On the screen shown below, click *Install* to continue.

6. Setup complete. Click *Finish* to restart the computer and for changes to take effect.
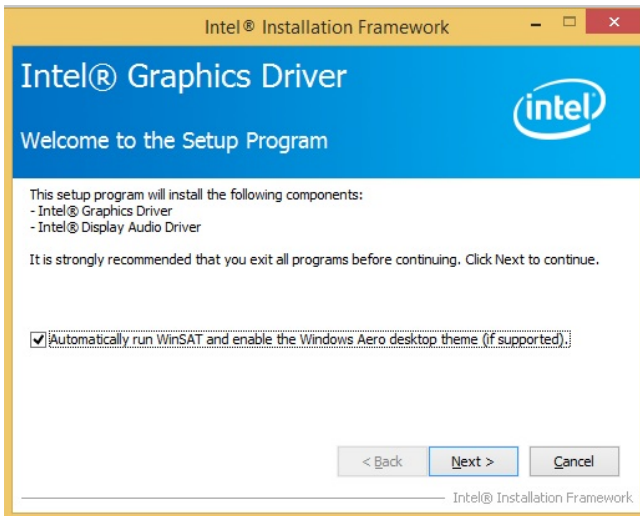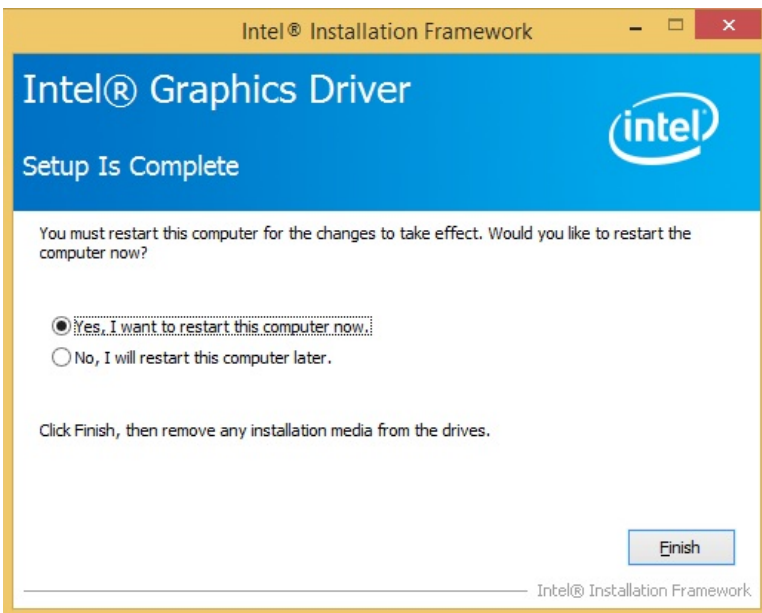
Realtek HD Audio Driver Installation

1. Insert the DVD that comes with the board. Click *Intel* and then *Intel(R) Skylake-U Chipset Drivers*.

2. Click *Realtek High Definition Audio Driver.*

3. On the Welcome to the InstallShield Wizard screen, click *Next* to proceed with and complete the installation process.

4. The InstallShield Wizard Complete. Click *Finish* to restart the computer and for changes to take effect.

LAN Drivers Installation

1. Insert the DVD that comes with the board. Click *Intel* and then *Intel(R) Skylake-U Chipset Drivers*.


2. Click *Intel(R) PRO LAN Network Driver.*

3. Click **Install Drivers and Software.**

4. When the Welcome screen appears, click **Next**.

5. Click *Next* to to agree with the license agreement.

6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.
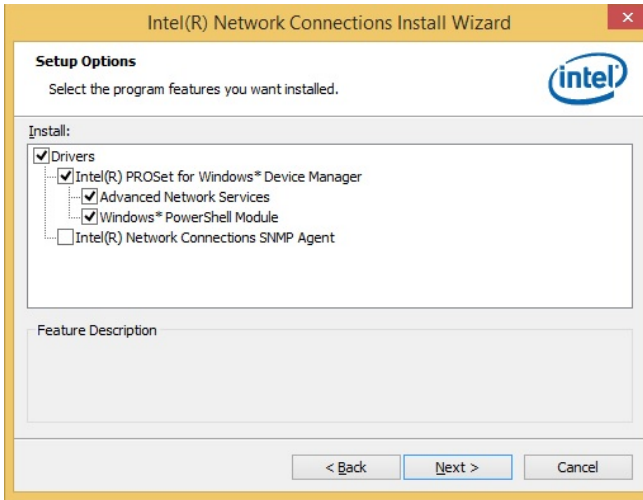
7. The wizard is ready to begin installation. Click *Install* to begin the installation.
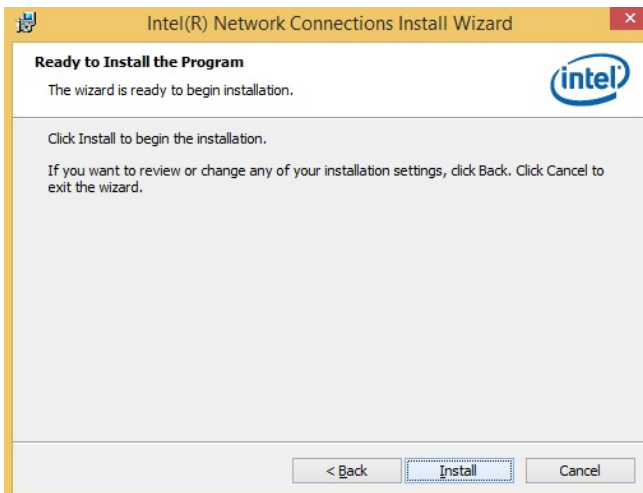
8. When InstallShield Wizard is complete, click *Finish*.

Intel® Management Engine Interface
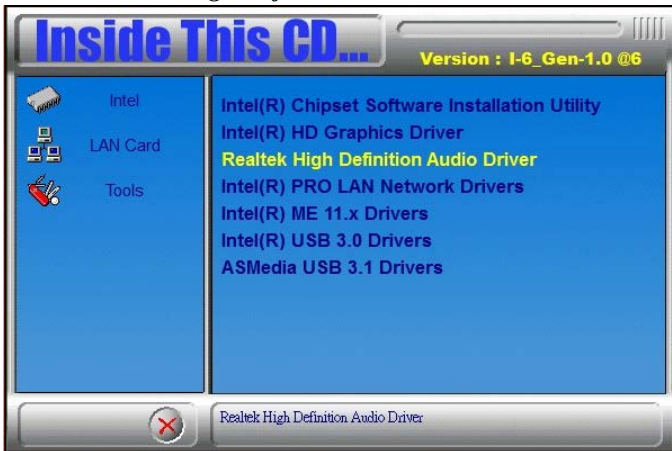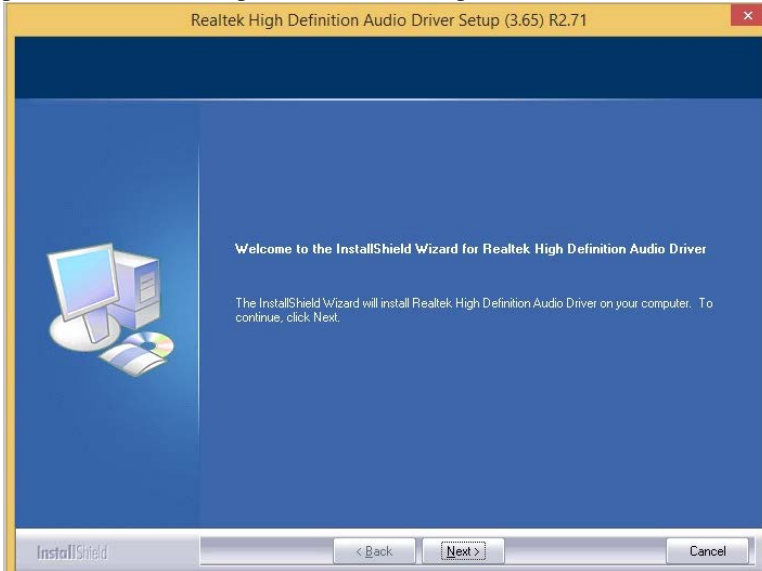
1. Insert the DVD that comes with the board. Click *Intel* and then *Intel(R) Skylake-U Chipset Drivers*.

2. Click *Intel (R) ME 11.x Drivers.*

3. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for **Install Intel® Control Center** & click *Next*.

4. Click *Next* to to agree with the license agreement.

5. When the Setup Progress screen appears, click *Next*. Then, click *Finish* when the setup progress has been successfully installed.

Intel® USB 3.0 Drivers

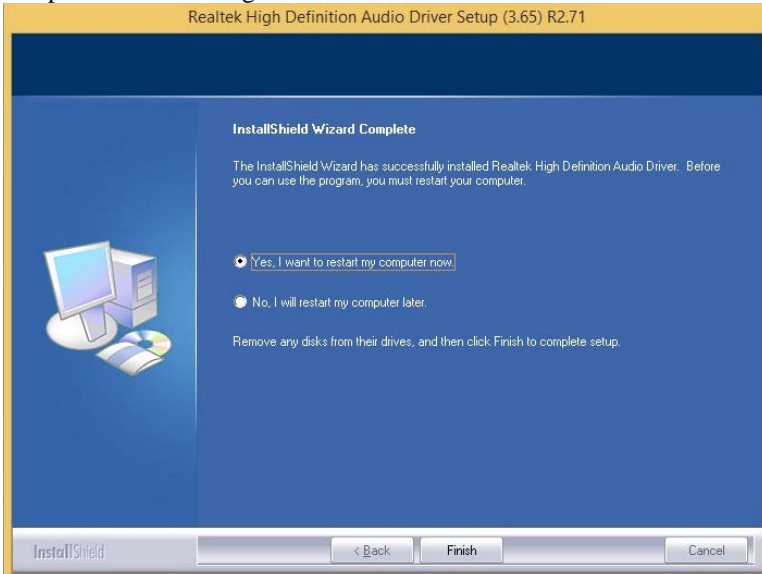1. Insert the DVD that comes with the board. Click *Intel* and then *Intel(R) Skylake-U Chipset Drivers*.

2. Click *Intel(R) USB 3.0 Drivers.*

3. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click *Next*.
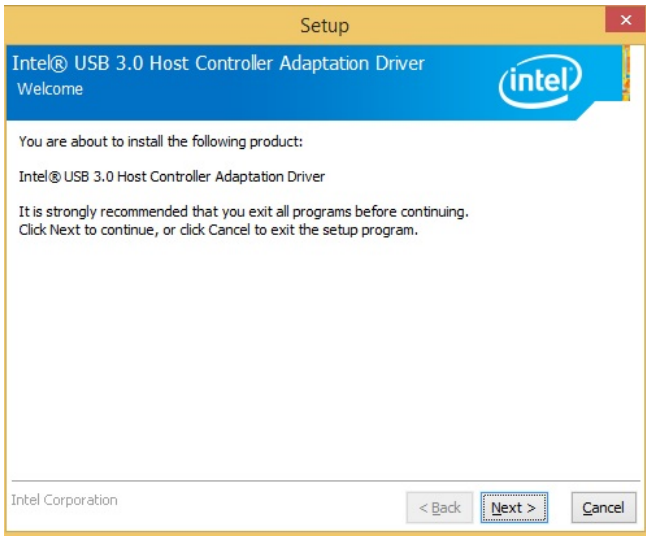
4. Click *Next* to agree with the license agreement and continue the installation.
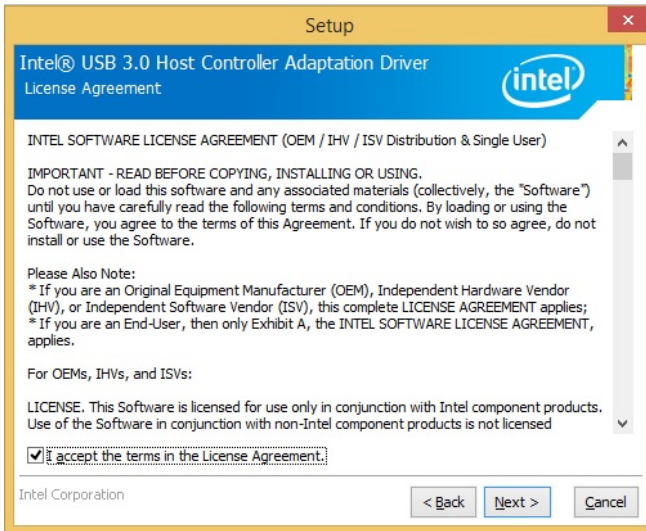
5. On the Readme File Information screen, click **Next** to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.

6. Setup complete. Click **Finish** to restart the computer and for changes to take effect.

ASMedia USB 3.1 Drivers
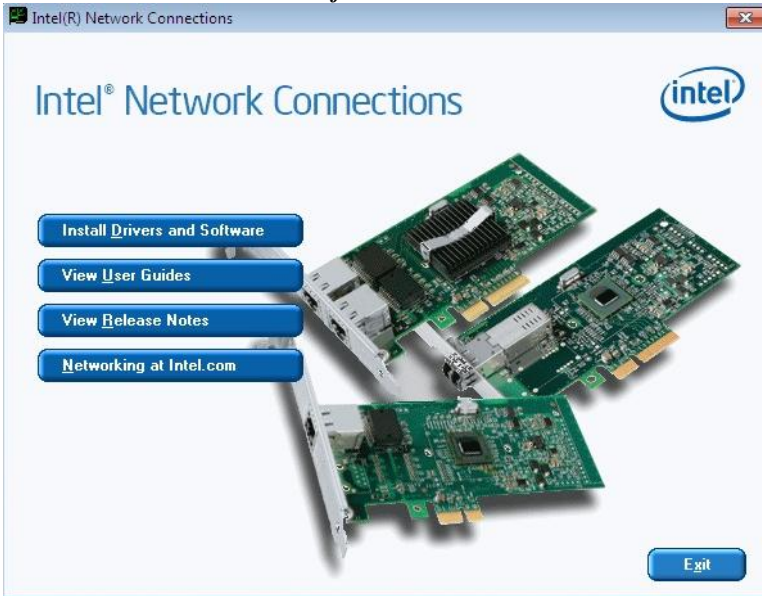
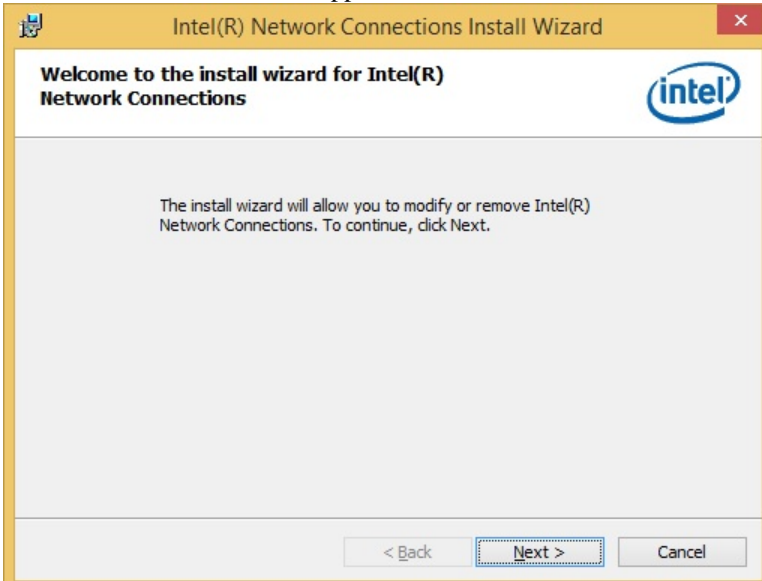1. Insert the DVD that comes with the board. Click *Intel* and then *Intel(R) Skylake-U Chipset Drivers*.


2. Click *ASMedia USB 3.1 Drivers.*

3. When the Welcome screen to the InstallShield Wizard for Asmedia USB Host Controller Driver, click *Next*.

4. Setup complete. Click *Finish*

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.
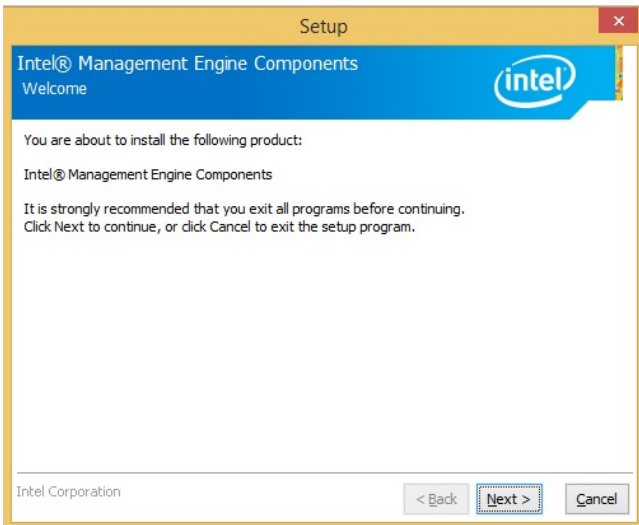
Address	Device Description
0000h-0CF7h	PCI Express Root Complex
0040h-0043h	System timer
0070h-0070h	System CMOS/real time clock
02E8h-02EFh	Fintek Communications Port (COM4)
02F8h-02FFh	Fintek Communications Port (COM2)
03E8h-03EFh	Fintek Communications Port (COM3)
03F8h-03FFh	Fintek Communications Port (COM1)
03B0h-03BBh	Intel(R) HD Graphics 520
03C0h-03DFh	Intel(R) HD Graphics 520
0D00h-FFFFh	PCI Express Root Complex

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer
IRQ1	Keyboard
IRQ3	Fintek Communications Port(COM2)
IRQ4	Fintek Communications Port(COM1)
IRQ7	Fintek Communications Port(COM3)
IRQ7	Fintek Communications Port(COM4)
IRQ11	Intel® Ethernet Connection I219-V
IRQ14	MotherBoard resources

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//-------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81866.H"
//-------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//-------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81866 watch dog program\n");

        SIO = Init_F81866();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81866, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }

        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime);  }
        else
        {       DisableWDT();          }

        return 0;
```

```
}
//-------------------------------------------------------------------------
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_F81866_Reg(0x2B);
        bBuf &= (~0x20);
        Set_F81866_Reg(0x2B, bBuf);                     //Enable WDTO

        Set_F81866_LD(0x07);                            //switch to logic device 7
        Set_F81866_Reg(0x30, 0x01);                     //enable timer

        bBuf = Get_F81866_Reg(0xF5);
        bBuf &= (~0x0F);
        bBuf |= 0x52;
        Set_F81866_Reg(0xF5, bBuf);                     //count mode is second

        Set_F81866_Reg(0xF6, interval);         //set timer

        bBuf = Get_F81866_Reg(0xFA);
        bBuf |= 0x01;
        Set_F81866_Reg(0xFA, bBuf);                     //enable WDTO output

        bBuf = Get_F81866_Reg(0xF5);
        bBuf |= 0x20;
        Set_F81866_Reg(0xF5, bBuf);                     //start counting
}
//-------------------------------------------------------------------------
void DisableWDT(void)
{
        unsigned char bBuf;

        Set_F81866_LD(0x07);                            //switch to logic device 7

        bBuf = Get_F81866_Reg(0xFA);
        bBuf &= ~0x01;
        Set_F81866_Reg(0xFA, bBuf);                     //disable WDTO output

        bBuf = Get_F81866_Reg(0xF5);
        bBuf &= ~0x20;
        bBuf |= 0x40;
        Set_F81866_Reg(0xF5, bBuf);                     //disable WDT
}
//-------------------------------------------------------------------------
```

```
//-----------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----------------------------------------------------------------------
#include "F81866.H"
#include <dos.h>
//-----------------------------------------------------------------------
unsigned int F81866_BASE;
void Unlock_F81866 (void);
void Lock_F81866 (void);
//-----------------------------------------------------------------------
unsigned int Init_F81866(void)
{
        unsigned int result;
        unsigned char ucDid;

        F81866_BASE = 0x4E;
        result = F81866_BASE;

        ucDid = Get_F81866_Reg(0x20);
        if (ucDid == 0x07)                              //Fintek 81866
        {       goto Init_Finish;       }

        F81866_BASE = 0x2E;
        result = F81866_BASE;

        ucDid = Get_F81866_Reg(0x20);
        if (ucDid == 0x07)                              //Fintek 81866
        {       goto Init_Finish;       }

        F81866_BASE = 0x00;
        result = F81866_BASE;

Init_Finish:
        return (result);
}
//-----------------------------------------------------------------------
void Unlock_F81866 (void)
{
        outportb(F81866_INDEX_PORT, F81866_UNLOCK);
        outportb(F81866_INDEX_PORT, F81866_UNLOCK);
}
//-----------------------------------------------------------------------
void Lock_F81866 (void)
{
        outportb(F81866_INDEX_PORT, F81866_LOCK);
}
//-----------------------------------------------------------------------
void Set_F81866_LD( unsigned char LD)
{
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, F81866_REG_LD);
        outportb(F81866_DATA_PORT, LD);
        Lock_F81866();
}
//-----------------------------------------------------------------------
void Set_F81866_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, REG);
        outportb(F81866_DATA_PORT, DATA);
        Lock_F81866();
}
//-----------------------------------------------------------------------
```

```
unsigned char Get_F81866_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, REG);
        Result = inportb(F81866_DATA_PORT);
        Lock_F81866();
        return Result;
}
//------------------------------------------------------------------------
```

```
//------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//------------------------------------------------------------------------
#ifndef __F81866_H
#define __F81866_H                      1
//------------------------------------------------------------------------
#define        F81866_INDEX_PORT        (F81866_BASE)
#define        F81866_DATA_PORT         (F81866_BASE+1)
//------------------------------------------------------------------------
#define        F81866_REG_LD            0x07
//------------------------------------------------------------------------
#define F81866_UNLOCK                   0x87
#define        F81866_LOCK              0xAA
//------------------------------------------------------------------------
unsigned int Init_F81866(void);
void Set_F81866_LD( unsigned char);
void Set_F81866_Reg( unsigned char, unsigned char);
unsigned char Get_F81866_Reg( unsigned char);
//------------------------------------------------------------------------
#endif //__F81866_H
```